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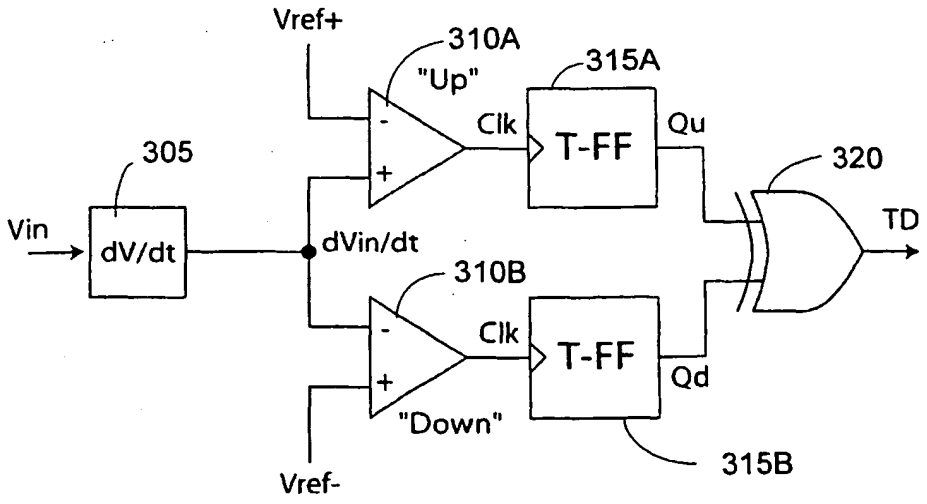


(57) Abstract: Clock recovery of a multi-level (ML) signal can be performed in a two-step process. First, the transitions within the ML signal can be detected by a novel transition detector (TD). And second, the output of the TD circuit can comprise a pseudo-non-return-to-zero (pNRZ) signal that can drive a conventional OOK clock recovery (CR) IC. The TD circuit can convert the edges of the ML signal into the pseudo-NRZ (pNRZ) signal. The TD circuit can capture as many transitions as possible to allow the conventional NRZ clock recovery (CR) chip to optimally perform. The TD circuit can differentiate the ML signal in order to detect the ML signal's transitions.

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# MULTI-LEVEL SIGNAL CLOCK RECOVERY TECHNIQUE

## PRIORITY AND RELATED APPLICATIONS

The present application claims priority to provisional patent application entitled, "MULTI-LEVEL SIGNAL CLOCK RECOVERY TECHNIQUE," filed on February 15, 2002 and assigned U.S. Application Serial No. 60/357,362. The entire contents of this provisional application are hereby incorporated by reference.

## TECHNICAL FIELD

The present invention relates to high speed communications. More particularly, the present invention relates to a system and method for recovering clock signals from multi-level signals in high speed optical and electrical communications.

## BACKGROUND OF THE INVENTION

In order to obtain increase spectral efficiency and therefore increased data throughput for both optical and electrical data transport systems, complex modulation schemes, such as multilevel (ML) signaling, are desired by the communications industry for both electrical and optical domain applications. Clock recovery of the resulting complex waveforms can be difficult, but is critical for data recovery.

Conventional telecommunication clock-recovery (CR) integrated circuits (IC's) are generally only designed for use with binary non-return-to-zero (NRZ) (or equivalently On-Off-Keyed, OOK, waveforms). Conventional CR IC's may employ comparators to determine the clock signal from the multi-level signal. Such an approach usually does not detect a high percentage of the transitions of a multilevel signal that are important to determine the clock signal.

Other conventional clock recovery units directly process multilevel signals to recover the clock signals. However, such units are not useful in the high speed communications environment because of the processing time needed by these conventional units to extract the clock signals from the multi-level signals.

In yet another conventional approach, processing of the multi-level signal is focused on the middle of the multi-level signal and not the edges of the signal. More precisely, the slopes and amplitudes at the temporal decision points of the multilevel signals are examined to align the recovered clock so as to minimize an estimated

sampling error. Such an approach focuses on minute signal amplitude variations, where the signal is expected to be flat, rather than major signal transitions, where the signal amplitude should generally experience major changes. The latter property is more indicative of the underlying clock. Also, usually in this conventional approach, the method involves decoding signal values prior to clock recovery. Such decoding is subject to decoding errors.

In view of the foregoing, there is a need in the art for efficiently detecting clock signals in a multilevel signal. There is a further need in the art for a system and method to determine clock signals from a multilevel signal in high speed communication applications.

## SUMMARY OF THE INVENTION

This invention offers an efficient method for recovering the clock or equivalently the symbol timing information of very high-speed ML waveforms. It can be particularly applicable to the clock recovery of ML signals within the receivers of high-speed telecommunication systems.

An ideal clock recovery approach usually synchronizes the rising (or falling) edge of the clock to the transitions of the ML signal. Signal transitions are usually defined as the process of the signal changing from one symbol (or level) to another.

Clock recovery of a multi-level signal can be performed in a two-step process. First, the transitions within the ML signal can be detected by a novel transition detector (TD). And second, the output of the TD circuit can comprise a pseudo-non-return-to-zero (pNRZ) signal that can drive a conventional OOK clock recovery (CR) IC. The NRZ signal is referred to as pNRZ because it can lack meaningful data content.

One objective of the TD circuit is to convert the edges of the signal into the pseudo-NRZ (pNRZ) signal for subsequent processing by a standard NRZ OOK clock recovery IC. It is desired to capture as many transitions as possible to allow the conventional NRZ clock recovery (CR) chip to optimally perform. In practice, NRZ clock recovery chips can lock to OOK NRZ data streams with reasonably diminished transition density (such as on the order of 1/10 to 1/100), but their locking performance can sometimes suffer.

An ideal transition detector can produce an output that inverts on every transition of the ML data stream. Since the pNRZ signal is generated in order to recover the clock, it is reasonable to assume that the clock does not exist for the TD function and therefore, the TD circuit is probably an analog and/or asynchronous function.

Another important feature of the present invention is that a ML signal Vin can be differentiated. This differentiated signal can be zero when the signal is flat (e.g. in the middle of the data symbol or when two adjacent symbols are the same) and large in magnitude when a transition occurs. Whether the derivative is positive or negative (corresponding to upward or downward transitions) can be immaterial since one objective of the present invention is simply to detect the transition and not its direction.

Consequently, the invention can threshold the absolute value of the derivative instead of the signed derivative, unlike many conventional clock recovery techniques known in the art that use the sign, positive or negative, of the slope around a nominal sampling point to determine whether a clock should be advanced or delayed.

The present invention evaluates the edges of the multi-level signals rather than flat regions in the center of the decision timing of the multi-level signals. And unlike conventional clock recovery techniques that require decoding of the multilevel signals prior to recovering the clock signal, the present invention can operate without decoding any of the multi-level signals prior to clock recovery. In other words, the present invention recovers clock signals with an analog process that is unlike many conventional clock recovery techniques that digitize multilevel signals prior to recovering any clock signals.

The present invention can use the derivative of the ML signal for detection of the ML signal's transitions. The ML input signal, Vin, can be differentiated in order to produce a waveform that can be labeled dVin/dt. The differentiated signal can drive two comparators with thresholds set to Vref+ and Vref-. The comparators can produce two outputs that can be labeled "Up" and "Down", which will become true as the signal, Vin, moves up or down, respectively.

When the signal rises, a positive derivative is present. The upper comparator with threshold set to Vref+ can assert an "Up" output. Similarly, when the input

signal falls, a negative derivative is present and the lower comparator can assert a "Down" output. These two outputs labeled "Up" and "Down" are then combined to produce the necessary pNRZ output.

The rising edges of the "Up" and "Down" signals can be "captured" with two toggle flip-flops (T-FF's). The T-FF's can simply invert their outputs on every rising edge from the comparators. The output of the T-FF's can be exclusive OR'ed (XOR'ed) together to produce the desired pNRZ signal. An XOR function will usually invert its output, if the state of either input changes provided the other input remains constant. Since Vin cannot move both up and down simultaneously, a rising edge occurring from either "Up" or "Down" will usually result in an inversion of the TD output. This can represent the ideal pNRZ signal generation as discussed above.

## BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of an exemplary multilevel clock recovery system according to an exemplary embodiment of the present invention.

Figure 2 is a block diagram illustrating some key functions of the transition detector circuit according to one exemplary embodiment of the present invention.

Figure 3 is a block diagram illustrating exemplary elements of the transition detector circuit according to one exemplary embodiment of the present invention.

Figure 4 is a series of graphs illustrating idealized waveforms for the operation of the exemplary transition detector circuit illustrated in Figure 3.

Figure 5 is a top-level schematic for an exemplary transition detector circuit shown in Figure 3.

Figure 6 is a block diagram of a series-C based differentiator circuit according to one exemplary embodiment of the present invention.

Figure 7 is a schematic of an exemplary differentiator circuit according one preferred exemplary embodiment of the present invention.

Figure 8 is a schematic diagram of an exemplary differential differentiator (DIFFDIFF) circuit according to one exemplary embodiment of the present invention.

Figure 9 is a schematic diagram of an exemplary current reference circuit according to one exemplary embodiment of the present invention.

Figure 10 is a series of graphs illustrating a simulation of the frequency response of the exemplary differentiator circuit illustrated in Figure 8.

Figure 11 a series of graphs illustrating simulated waveforms for the operation of an exemplary transition detector circuit according to one exemplary embodiment of the present invention.

Figure 12 is a diagram illustrating a waveform for the derivative threshold point in an exemplary transition detector circuit according to exemplary embodiment of the present invention.

Figure 13 is an illustration of a simulated eye-diagram and output diagram for an exemplary transition detector circuit according to one exemplary embodiment of the present invention.

Figure 14 is a series of graphs illustrating the deterministic jitter that can be introduced by the transition detection method illustrated Figure 3.

Figure 15 is a block diagram of illustrating a detection method to remove deterministic jitter according to one exemplary embodiment of the present invention.

Figure 16 is a block diagram illustrating a more detailed version of the detection method illustrated in Figure 15..

Figure 17 is a block diagram illustrating a more detailed and exemplary implementation of the modules illustrated in Figure 16.

## DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

Clock recovery of a multi-level (ML) signal can be performed in a two-step process. First, the transitions within the ML signal can be detected by a novel transition detector (TD). And second, the output of the TD circuit can comprise a pseudo-non-return-to-zero (pNRZ) signal that can drive a conventional OOK clock recovery (CR) IC. The TD circuit can convert the edges of the ML signal into the pseudo-NRZ (pNRZ) signal. The TD circuit can capture as many transitions as possible to allow the conventional NRZ clock recovery (CR) chip to optimally perform. The TD circuit can differentiate the ML signal in order to detect the ML signal's transitions.

An exemplary transition detection circuit has been built by the inventors and simulated to operate at 2.7 Giga Symbols per second (Gsym/sec) in a Gallium

Arsenide (GaAs) heterojunction bi-polar transistor (HBT) process. In other words, the inventors have fabricated a working model of the present invention. The present invention can also be readily adapted to a variety of other semiconductor processes such as Complimentary Metal Oxide Semiconductor (CMOS) or Silicon Germanium (SiGe) as is apparent to one of ordinary skill in the art.

Referring now to the drawings, in which like numerals represent like elements throughout the several Figures, aspects of the present invention and the illustrative operating environment will be described.

Referring to Figure 1, this Figure is a block diagram of an exemplary multilevel clock recovery system 100 according to an exemplary embodiment of the present invention. The clock recovery system 100 can comprise a transition detector (TD) 105 and a conventional clock recovery unit (CR) 110 that can process OOK type signals. The output of the TD circuit 105 can comprise a pseudo-non-return-to-zero (pNRZ) signal that can drive the conventional OOK clock recovery (CR) IC 110. The NRZ signal is referred to as pNRZ because it can lack meaningful data content.

Referring now to Figure 2, this Figure is a block diagram illustrating some key functions of the transition detector circuit 105 according to one exemplary embodiment of the present invention. The transition detector circuit 105 can comprise three stages: a derivative stage 205, an absolute value of the derivative stage 210, and a threshold comparison stage 215.

Referring now to Figure 3, this Figure is a block diagram illustrating exemplary elements of the transition detector circuit 105 according to one exemplary embodiment of the present invention. The ML input signal, Vin, can be differentiated by a differentiator 305 in order to produce a waveform that can be labeled dVin/dt. The differentiated signal can drive two comparators 310A, 310B with thresholds set to Vref+ and Vref-. The comparators 310A, 310B can produce two outputs that can be labeled "Up" and "Down", which will become true as the signal, Vin, moves up or down, respectively.

When the signal rises, a positive derivative is present. The upper comparator 310A with threshold set to Vref+ can assert an "Up" output. Similarly, when the input signal falls, a negative derivative is present and the lower comparator 310B can

assert a "Down" output. These two outputs labeled "Up" and "Down" are then combined via an exclusive "OR" function 320 to produce the necessary pNRZ output.

The rising edges of the "Up" and "Down" signals can be "captured" with two toggle flip-flops (T-FF's) 315A, 315B. The T-FF's 315A, 315B simply invert their outputs on every rising edge from the comparators. The output of the T-FF's 315A, 315B can be exclusive OR'ed (XOR'ed) together at 320 to produce the desired pNRZ signal. An XOR function 320 will invert its output, if the state of either input changes provided the other input remains constant. Since Vin cannot move both up and down simultaneously, a rising edge occurring from either "Up" or "Down" will result in an inversion of the TD output. This can represent an ideal pNRZ signal generation.

Referring now to Figure 4, this Figure is a series 400 of seven graphs 405-435 illustrating idealized waveforms for the operation of the exemplary transition detector circuit 105 illustrated in Figure 3. The first graph 405 illustrates the multilevel signal input into the transition detector circuit 105.

The second graph 410 illustrates a derivative of the multilevel signal from the first graph 405. The third graph 415 illustrates an output of the first comparator 310A. Meanwhile, the fourth graph 420 illustrates an output of the second comparator 310B. The fifth graph 425 illustrates an output of the first toggle flip-flop 315A. And the sixth graph 430 illustrates an output of the second toggle flip-flop 315B. The seventh graph 435 illustrates the output of the exclusive "or" function 320.

Figure 5 illustrates the top-level schematic for the exemplary transition detector illustrated in Figure 3. The circuit is a fully differential design and is functionally identical to the block diagram of Figure 3. The differentiation function is performed by the circuit block labeled DIFFDIFF (X13) (differential differentiator). The differentiated signal is amplified by a simple differential limiting amplifier, X17.

The differential output of the limiting amplifier is routed to two differential comparators that have thresholds set by the voltages at the input pins Vrdp, Vrdm, and the common reference pin Vr. The differential outputs from the comparators toggle two T-FF's that are made from two D-FF's (X4 and X11). The differential outputs of the FF's are XOR'ed by a differential XOR gate, X12. Finally, the output of the XOR

gate is buffered by an OUTBUF circuit, which provides appropriate drive for the OOK CR IC.

The differential differentiator circuit employs a novel approach as described below. Differentiation can be accomplished by a variety of methods. An exemplary differential differentiator 305' is illustrated in Figure 6. In this approach an amplifier, A1, with a low output impedance, drives a series-connected RC network. The resistor R combined with the output impedance of the amplifier must be low enough to force an accurate representation of the input signal across the capacitor. Then, the resulting current through the capacitor will be the derivative of the input voltage (with a possible gain/loss factor). That is, for an ideal capacitor:

$$I = C\frac{dV}{dt}. \tag{1}$$

The voltage across the resistor, R, will be directly proportional to this current (Ohm's law). Therefore, if the input amplifier has a gain G1 and the output amplifier a gain G2, the circuit's transfer function will be:

$$V_{out} = G1\,G2\,R\,C\frac{dV_{in}}{dt} \tag{2}$$

provided that the input voltage is appropriately impressed across the capacitor, C. In order for the input voltage to appear across the capacitor, the RC cutoff frequency must be much greater than the operating frequency:

$$f_{op} << \frac{1}{2\pi C(R + R_{out1})}, \tag{3}$$

in which $R_{out1}$ is the output impedance of amplifier A1; and A2 is assumed to have a high input impedance. Equation (3) indicates that the RC product must be small for high frequency operation ($f_{op}$).

Therefore, the amplifier gains, G1 and G2, must be large to offset the signal loss as per Equation (2). The approach illustrated in Figure 6 and described above is not a preferred exemplary embodiment because useful circuit function requires large gain and/or a low impedance amplifier to drive the RC network.

Referring now to Figure 7, a preferred and exemplary embodiment of an exemplary differentiator 305" is illustrated in Figure 7. For this exemplary embodiment, a shunt capacitor C is directly connected to the output of a low impedance emitter follower 705. The relevant RC time constant is simply the output

resistance of the emitter follower 705 and the capacitance, C. Since the output impedance of an emitter follower can be designed to be very low, the RC bandwidth for impressing the voltage across the capacitor C can be very high.

The emitter follower 705 is further designed to have a collector resistance from which the output is derived. The capacitor, C, is charged through the transistor 710 and therefore the current through $R_{out}$ is an identical representation (ignoring the transistor's finite $\beta$ and an offset current) of the current in the capacitor C. By inspection, the output voltage, Vout, is as follows:

$$V_{out} \cong -RI_o - R_{out}C\frac{d(V_{in} - V_{off})}{dt} \quad (4)$$

where $I_o$ is the DC bias current and $V_{off}$ is an input offset due primarily to $V_{be}$. An important aspect of Equation (4) is that $R_{out}$ can be set arbitrarily large (determined by the subsequent circuit load) so that the circuit can represent significant gain as compared to the basic conventional approach described earlier.

The offsets involved in Equation (4) are undesirable, but they are both approximately constant. The variable $I_o$ is set by a current source and $V_{off}$ is approximately $V_{be}$. Additionally, a fully differential design, as described below, eliminates these offsets.

Referring now to Figure 8, a transistor level schematic diagram of an exemplary differentiator circuit (DIFFDIFF) 800 is illustrated. This circuit, though complex at first inspection, generally comprises two of the basic circuits shown in Figure 7 operated differentially. The input is first differentially buffered by the differential input amplifier comprising X13 and X14. The differential outputs of this amplifier drive two emitter follower stages (each) comprising X11, X16 and X17, X9. The low impedance output of the emitter followers accurately impresses the input voltage across capacitors C3 and C2. These capacitors could be replaced by one differentially connected capacitor between the two emitter follower outputs. Such a connection assumes perfect symmetry of the amplifiers, and simulation suggests improved operation by using the equivalent split capacitor approach as shown. The resistors R23 and R24 were added to help stabilize the emitter follower amplifiers – it is well known that capacitive loads can cause instabilities with emitter follower amplifiers. The differential output is obtained from the collector resistors R9 and R1.

Referring now to Figure 9, this figure illustrates exemplary current reference circuit 900 used to control the bias of the differential differentiator circuit. This circuit can comprise a "Beta-helper"- type current reference source. In other words, this circuit 900 provides a current reference for all of the current sources at bottom of Figure 8.

Specifically, the current reference source circuit 900 can provide current for the lowest row of transistors illustrated in Figure 8. The present invention is not limited to this type of current reference source 900 illustrated in Figure 9. Other current reference source circuits are known in the art and are not beyond the scope and spirit of the present invention.

Referring now to Figure 10, a significant issue with the use of differentiators is that they have a frequency response that increase linear with frequency. This has a tendency to amplify noise of the input signal. Therefore, a differentiator should ideally only operate over a bandwidth that matches the input signal. Figure 10 illustrates a simulation 1000 of the frequency response of the differentiator circuit. The ideal frequency response of a differentiator is simply $j\omega$ (The Fourier transform of dV/dt is jωF(V)). The simulation in Figure 10 shows a linear amplitude response up to approximately 2 GHz with a linear phase response starting at 90 degrees as expected at low frequencies.

The linear slope of the phase response is simply due to the delay through the circuit and has no consequence for normal operation (The Fourier transform of a time delay is a linear phase offset). The response is seen to peak at slightly over 3 GHz and was observed to roll off gracefully at higher frequencies.

Referring now to Figure 11, this Figure illustrates a result of a simulation of the complete TD circuit driven 105 by an ML signal. Figure 11 includes a series of graphs 1100 that are similar to the graphs of Figure 4. However, Figure 11 illustrates a simulated multi-level signal instead of an idealized multilevel signal that is illustrated in Figure 4.

Figure 11 also demonstrates that the transition circuit 105 catches almost all transitions as predicted. The first graph 1105 illustrates the multilevel signal input into the transition detector circuit 105.

The second graph 410 illustrates a derivative of the multilevel signal from the first graph 1105. The third graph 1115 illustrates an output of the first comparator 310A. Meanwhile, the fourth graph 1120 illustrates an output of the second comparator 310B. The fifth graph 1125 illustrates an output of the first toggle flip-flop 315A. And the sixth graph 1130 illustrates an output of the second toggle flip-flop 315B. The seventh graph 1135 illustrates the output of the exclusive "or" function 320.

Referring now to Figure 12, this figure illustrates detail of the comparator process. In other words, this Figure illustrates a waveform 1200 and the derivative threshold points 1205, 1210 according to an exemplary transition detector circuit 105.

Referring now to Figure 13, this Figure is a series of graphs that summarizes the overall circuit performance of the transition detection circuit 105. The first graph 1305 comprises an eye diagram of the TD output that will be fed to an OOK CR chip. Reasonable jitter width is observed and much of this jitter can be suppressed by the subsequent OOK CR IC's jitter rejection properties. The second graph 1310 illustrates the output of the transition detection circuit 105.

From Figure 13, one skilled in the art will recognize that the recovered signal, while giving a better result than without the use of the TD, exhibits what is known as deterministic jitter (DJ). DJ is temporal variability in the transition location due to patterns in the data sequence.

Figure 14 illustrates the source of this DJ. Figure 14(a) illustrates an exemplary eye-diagram 1405 of a ML signal with 16 levels. Figure 14(b) illustrates exemplary corresponding absolute values 1410 of the derivatives of the signals illustrated in Figure 14(a). The only difference among the fifteen derivatives in Figure 14(b) is their amplitude, i.e. they are all scalings of a single function. The dashed horizontal line 1415 in Figure 14(b) illustrates the transition threshold Vref used.

The location where this horizontal line crosses a particular derivative is a respective declared transition point 1420A, 1420B. While only two declaration transition points 1420A, 1420B are labeled in Figure 14(b), those skilled in the art will appreciate that thirteen additional declarations transition points are not labeled but do exist and correspond to the remaining thirteen derivatives.

As is evident from Figure 14(b), this declaration point occurs earlier for larger level transitions. Due to this variability, jitter is introduced by the TD circuit and can degrade performance of subsequent circuitry making use of the recovered clock. While CR following the TD circuit will reduce this DJ, the CR may not be able to remove all the DJ. Furthermore, in the presence of additional random jitter and DJ from other sources, the CR may not be able to fully compensate for their aggregate effect.

The DJ illustrated in Figure 14 is due to sensitivity to data patterns. It is important to note that the DJ is not due to noise. Thus, it is theoretically possible to remove the DJ with appropriate methods. Figure 15 shows a block diagram extending the functionality in Figure 2 to remove DJ. The constant threshold transition detection (CTTD) of Figure 2 is actually included as a subset of Figure 15.

The embodiment illustrated in Figures 15 through 17 will be called the variable threshold transition detection (VTTD) circuit. The new function blocks are used to provide the CTTD with a variable threshold that scales with the size of the level change. This effectively normalizes the threshold thereby eliminating the inconsistency illustrated in Figure 14(b).

Referring now to Figure 15, this Figure illustrates a variable threshold obtained by comparing a multi-level signal at different points in time. In particular, the signal Vin is delayed by an amount $\tau$ twice, splitting the signal off after each delay. This provides three instances of the signal: $Vin(t+\tau)$, $Vin(t)$, and $Vin(t-\tau)$. If $\tau$ is chosen to be on the order of half a symbol period (note that exactness in the value of $\tau$ is not necessary), then $Vin(t+\tau)$ and $Vin(t-\tau)$ will correspond to the middle of the data symbols for the preceding and following symbols when $Vin(t)$ is in the transition region. Thus, the difference $Vin(t+\tau)-Vin(t-\tau)$ provides a good estimate of the size of the level change. Scaling this difference by an appropriate factor $\alpha$ (where $\alpha$ is nominally 1/2 in the absence of gain on circuit elements) provides the desired threshold on a continuous basis.

The difference $Vin(t+\tau)-Vin(t-\tau)$ in Figure 15 is difficult to implement as illustrated. However, because the difference is only used by the threshold operation, which is implemented with comparators as in Figure 3, this difference never need be explicitly performed.

Referring now to Figures 16 and 17, these Figures present an embodiment that functionally implements Figure 15 but without explicitly taking the difference $Vin(t+\tau)-Vin(t-\tau)$. For clarity of exposition, Figure 16 presents the embodiment in higher-level function blocks whose specifics are given in Figure 17.

As in Figure 15, three instances of Vin are created by the use of a pair of $\tau$ delays. The middle tap Vin(t) is differentiated according to the embodiment previously described for the CTTD and scaled by $1/\alpha$. Note that Vin(t) is scaled by $1/\alpha$, in contrast to scaling $Vin(t+\tau)$ and $Vin(t-\tau)$ by $\alpha$, to save on the number of amplifiers used. However, both approaches are inherently the same and are represented by the same embodiment.

The three signals $Vin(t+\tau)$, $1/\alpha$ Vin(t), and $Vin(t-\tau)$ are then fed into three modules. The first module (i) tests if the derivative dVin(t)/dt of the ML signal is greater than the threshold $\alpha|Vin(t+\tau)-Vin(t-\tau)|$.

The second module (ii) tests if the derivative dVin(t)/dt is less than the threshold $-\alpha|Vin(t+\tau)-Vin(t-\tau)|$. The 'OR'ing of these two events then corresponds to the absolute value of the derivative exceeding $|\alpha[Vin(t+\tau)-Vin(t-\tau)]|$ and thus conveys when the slope of the ML signal has exceeded the variable threshold.

The third module (iii) asserts a minimum value on the slope threshold. Note that when two adjacent symbols are the same, the variable threshold becomes zero, and modules (i) and (ii) will trigger. Module (iii) safeguards against such conditions causing a "false alarm" by additionally requiring the slope reach a minimum threshold in order to accept the results of modules (i) and (ii). While module (iii) asserts a slope on the derivative dVin(t)/dt, those skilled in the art will recognize that applying a threshold to the difference $[Vin(t+\tau)-Vin(t-\tau)]$ is fundamentally the same embodiment.

Figure 17 illustrates the details of each of the modules (i)-(iii) in Figure 16. Figure 17(top) shows how module (i) can be implemented. As in Figure 16, module (i) takes as its input $Vin(t-\tau)$, $1/\alpha\ Vin(t)$, and $Vin(t+\tau)$. To implement the desired function, we note that the event

$$dVin(t)/dt > |\alpha[Vin(t+\tau)-Vin(t-\tau)]|$$

is equivalent to the pair of events being true

$$1/\alpha\ dVin(t)/dt + Vin(t-\tau) > Vin(t+\tau)$$

$$1/\alpha\ dVin(t)/dt + Vin(t+\tau) > Vin(t-\tau)$$

as can be shown by those skilled in the art. The latter pair of conditions can be directly implemented as shown in Figure 17(top) to produce the desired functionality.

In a similar fashion, module (ii) can be implemented as in Figure 17(middle) taking advantage of the equivalence of the event

$$dVin(t)/dt < -|\alpha[Vin(t+\tau)-Vin(t-\tau)]|$$

to the pair of events

$$1/\alpha\ dVin(t)/dt + Vin(t-\tau) < Vin(t+\tau)$$

$$1/\alpha\ dVin(t)/dt + Vin(t+\tau) < Vin(t-\tau)$$

being true. It should be evident to those skilled in the art that two of the four additions in modules (i) and (ii) are redundant and can be omitted. As previously stated, the separation of functionality into modules is for clarity of exposition and not an implementation constraint.

Finally, for third module (iii), the minimum threshold requirement can be realized with the implementation shown in Figure 17(bottom) where the ML signal derivative is compared to the threshold Tmin. As in Figure 3, a pair of thresholds is used to account for both when the derivative is positive and negative. The two comparators are then latched and 'OR'ed to produce the desired output.

The present invention efficiently detects clock signals in a multilevel signal. The system and method of the present invention determine clock signals from a multilevel signal that can be used in high speed communication applications. Exemplary uses of the present invention include electrical backplane, Ethernet, and optical applications.

It should be understood that the foregoing relates only to illustrate the embodiments of the present invention, and that numerous changes may be made

therein without departing from the scope and spirit of the invention as defined by the following claims.

# CLAIMS

What is Claimed is:

1. A system for determining a clock signal from a multi-level signal comprising:

a transition detector for differentiating a multi-level signal to form a differentiated signal that enables detection of edges of the multi-level signal and for generating a binary signal based on the differentiated signal; and

a clock recovery unit for receiving the binary signal and determining a clock signal, whereby increased data transitions are realized from the multilevel signal and time for determining the clock signal and jitter are reduced.

2. The system of Claim1, wherein the transition detector splits the differentiated signal into a first differentiated signal and a second differentiated signal.

3. The system of Claim 2, wherein the transition detector thresholds the first differentiated signal against a predetermined value for detecting magnitudes of the first differentiated signal above the predetermined value.

4. The system of Claim 2, wherein the transition detector thresholds the second differentiated signal against a predetermined value for detecting magnitudes of the second differentiated signal below the predetermined value.

5. The system of Claim 1, wherein the transition detector splits the differentiated signal into two differentiated signals, and thresholds the two differentiated signals to detect upward and downward transitions, converts each of the two return-to-zero thresholded signals into a non-return-to-zero signal, and combines the two non-return-to-zero signals together to convey both upward and downward transitions in a single signal .

6. The system of Claim 1, wherein the transition detector comprises a differentiator circuit.

7. The system of Claim 1, wherein the transition detector comprises a comparator and a toggle flip flop.

8. The system of Claim 1, wherein the transition detector comprises a shunt capacitor connected to an output of a low impedance emitter or source of a transistor.

9. A system for receiving a multi-level signal and determining a clock signal from the multi-level signal comprising:

a variable threshold transition detector for differentiating a multilevel signal to form a signal that enables detection of edges of the multi-level signal, for sampling the signal at different points in time and applying an adaptive threshold to the differentiated signal to form a thresholded signal, and for generating a binary signal based on the thresholded signal;

a clock recovery unit for receiving the binary signal and determining a clock signal, whereby increased data transitions are realized from the multilevel signal and the period of time for determining the clock signal and jitter are reduced.

10. The system of Claim 9, wherein the variable threshold transition detector determines if a magnitude of a derivative based on the multilevel signal is greater than a predetermined threshold value.

11. The system of Claim 9, wherein the variable threshold transition detector determines if a magnitude of a derivative based on the multilevel signal is less than a predetermined threshold value.

12. The system of Claim 9, wherein the variable threshold transition detector splits the multilevel signal into two signals, differentiates the two signals, thresholds the differentiated signals against two predetermined values, and combines the thresholded signals into one signal.

13. The system of Claim 12, wherein the variable threshold transition detector combines the thresholded signals into one signal by using one of an exclusive-or (XOR) and logical-or (OR) operation between the two signals.

14. The system of Claim 9, wherein the variable threshold transition detector delays and splits the multilevel signal into at least two delayed signals, and differentiates and splits one of the delayed signals.

15. The system of Claim 9, wherein the variable threshold transition detector delays and splits the multilevel signal into three delayed signals, differentiates one of the three delayed signals, and combines the signals back into one signal for further processing by the clock recovery unit.

16. A method for identifying a clock signal from a multi-level signal comprising:

receiving a multi-level signal;

differentiating the multi-level signal to form a differentiated signal;

detecting edges of the multilevel signal by thresholding the differentiated signal;

generating a binary signal based on the differentiated signal; and

identifying a clock signal from the binary signal, whereby increased data transitions are realized from the multilevel signal and a period of time for determining the clock signal and jitter are reduced.

17. The method Claim 16, further comprising splitting the differentiated multi-level signal into a first differentiated signal and a second differentiated signal.

18. The method of Claim 17, wherein thresholding the differentiated signal comprises comparing the first differentiated signal to a predetermined value for detecting magnitudes of the first differentiated signal above the predetermined value.

19. The method of Claim 17, wherein thresholding the differentiated signal comprises comparing the second differentiated signal against a predetermined value for detecting magnitudes of the second differentiated signal below the predetermined value.

20. The method of Claim 16, further comprising splitting the differentiated signal into two differentiated signals, thresholding the two differentiated signals to form two return-to-zero thresholded signals, converting the two return-to-zero thresholded signals into two non-return-to-zero signals, and combining the two non-return-to-zero signals back together.

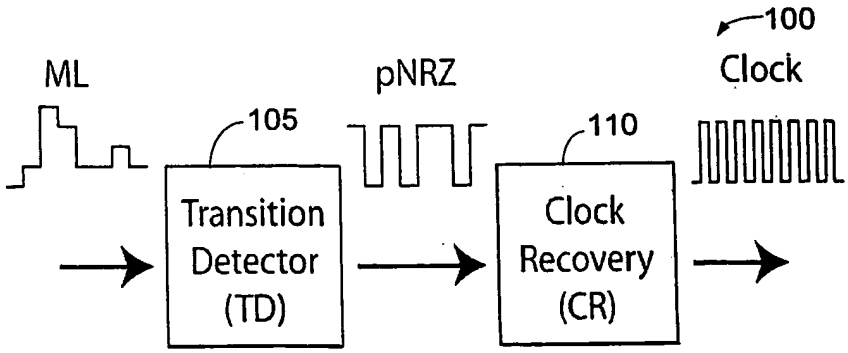


FIG. 1

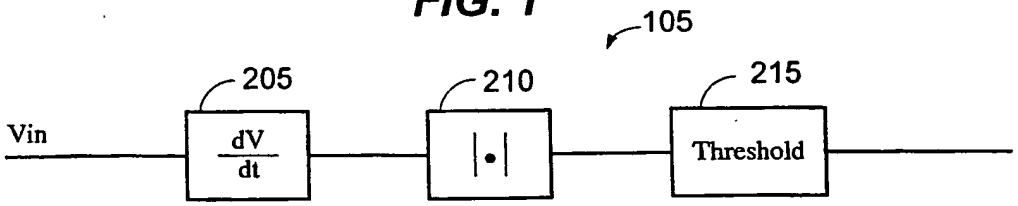


FIG. 2

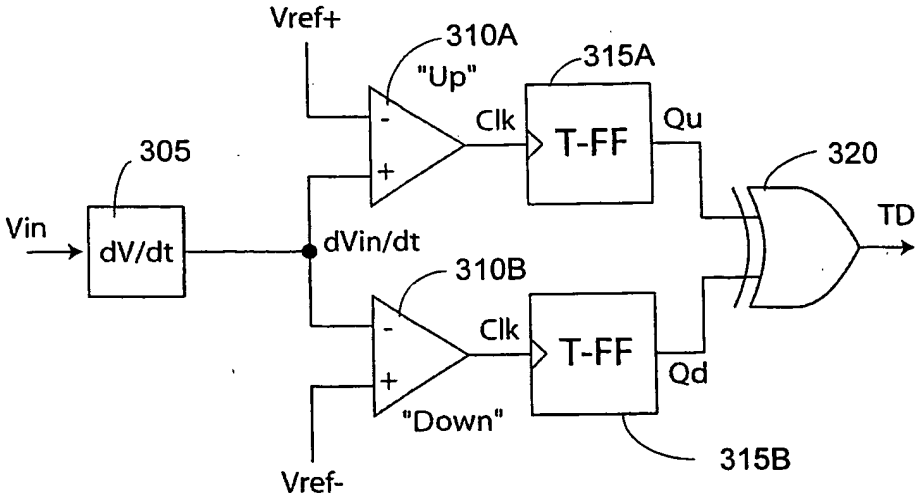


FIG. 3

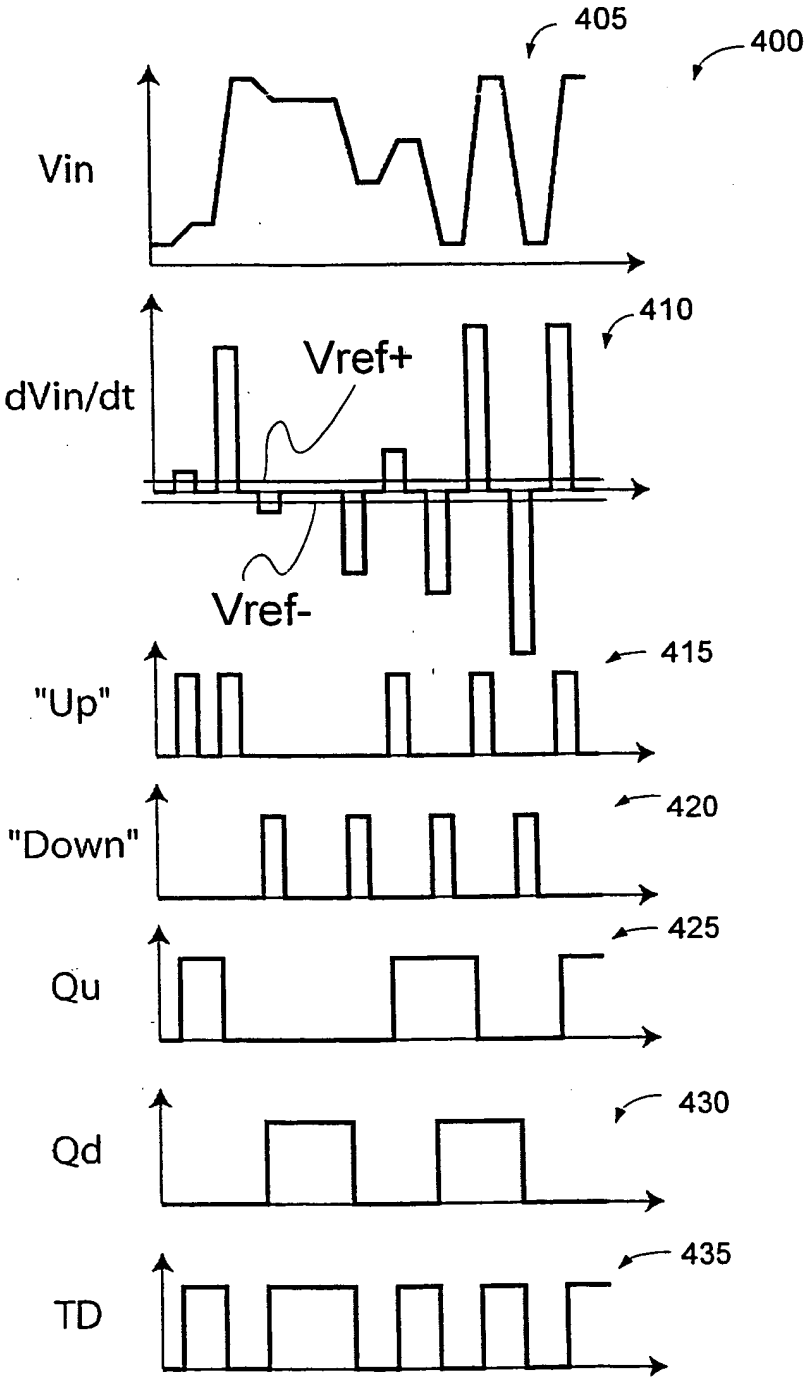
405
400
Vin
410
dVin/dt
Vref+
Vref-
415
"Up"
420
"Down"
425
Qu
430
Qd
435
TD

*FIG. 4*

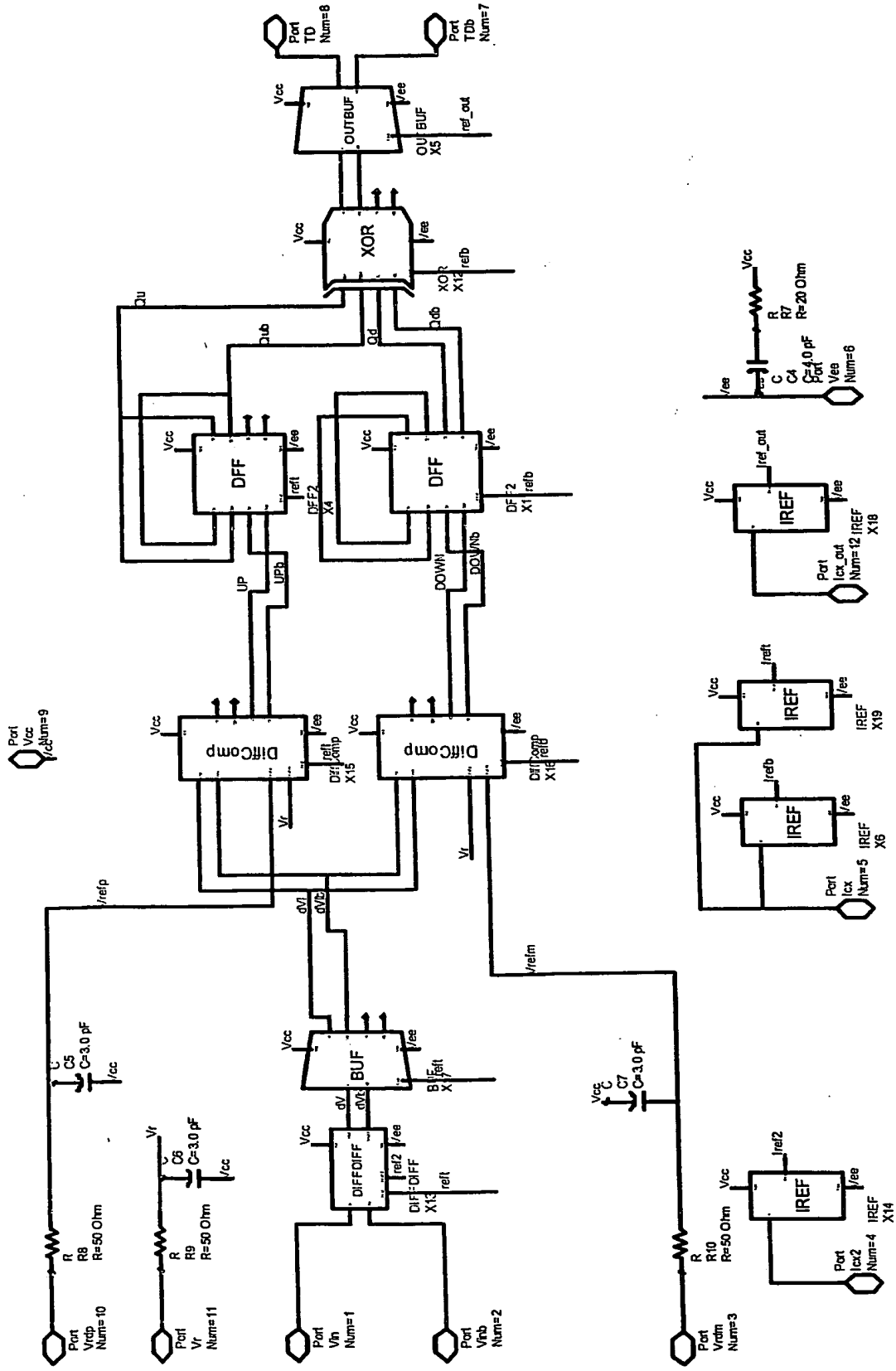
Port TD Num=8
Port TDb Num=7
OUTBUF
OUTBUF X5
ref_out
XOR
XOR X12
refb
Qu
Qub
Qd
Qdb
DFF
DFF2 X4
DFF2 X1
reft
UP
UPb
DOWN
DOWNb
DiffComp
Diff_comp X15
Diff_comp X16
Vr
Vcc
Vee
Vrefp
Vrefm
dV1
dV1b
BUF
BUF X7
DIFFDIFF
DIFF_DIFF X13
ref2
C5 C=3.0 pF
C6 C=3.0 pF
C7 C=3.0 pF
R8 R=50 Ohm
R9 R=50 Ohm
R10 R=50 Ohm
R7 R=20 Ohm
C4 C=4.0 pF
Port Vrdp Num=10
Port Vr Num=11
Port Vrn Num=1
Port Vrb Num=2
Port Vrdm Num=3
Port Vee Num=6
IREF
IREF X18
IREF X19
IREF X6
IREF X14
Port Icx_out Num=12
Port Icx Num=5
Port Icx2 Num=4

Fig. 5

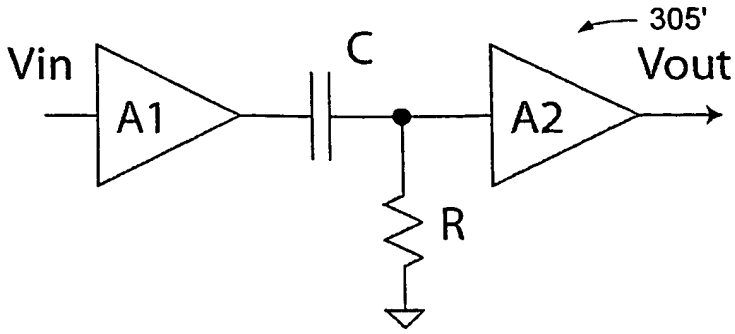


FIG. 6

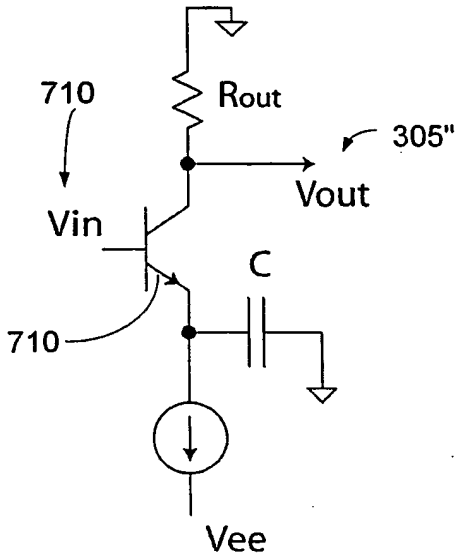


FIG. 7

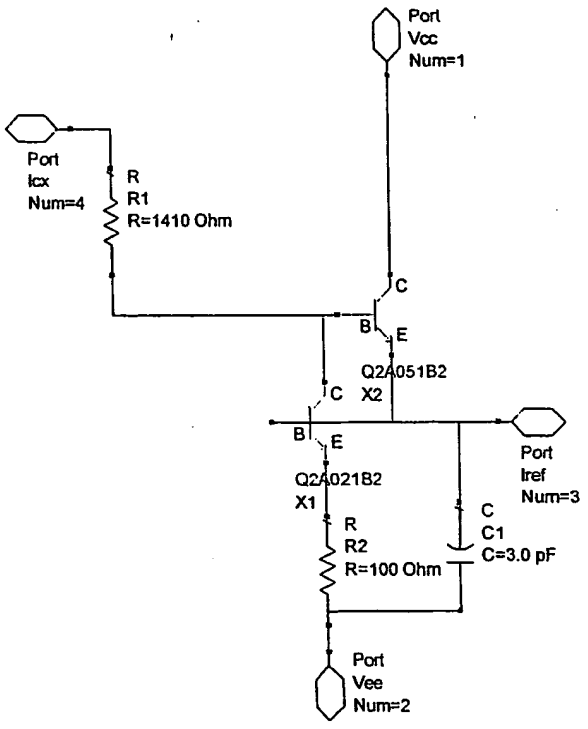


FIG. 9

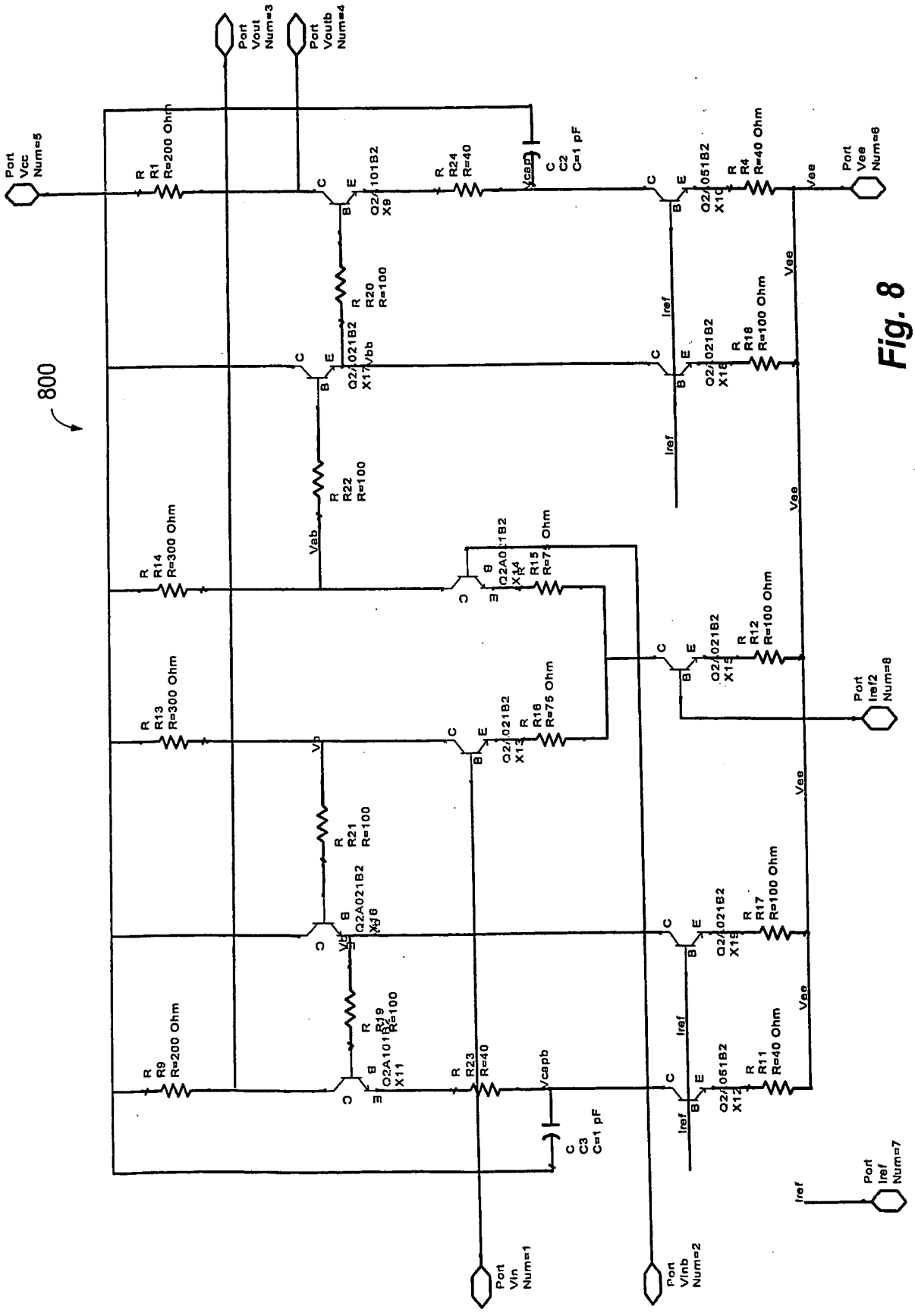
800
Port Vout Num=3
Port Voutb Num=4
Port Vcc Num=5
Port Vee Num=6
Port Iref2 Num=8
Port Iref Num=7
Port Vin Num=1
Port Vinb Num=2
R R1 R=200 Ohm
R R4 R=40 Ohm
R R9 R=200 Ohm
R R11 R=40 Ohm
R R12 R=100 Ohm
R R13 R=300 Ohm
R R14 R=300 Ohm
R R16 R=75 Ohm
R R17 R=100 Ohm
R R18 R=100 Ohm
R R20 R=100
R R21 R=100
R R22 R=100
R R23 R=40
R R24 R=40
C C2 C=1 pF
C C3 C=1 pF
Vcapb
Vab
Vb
Iref
Vee

Fig. 8

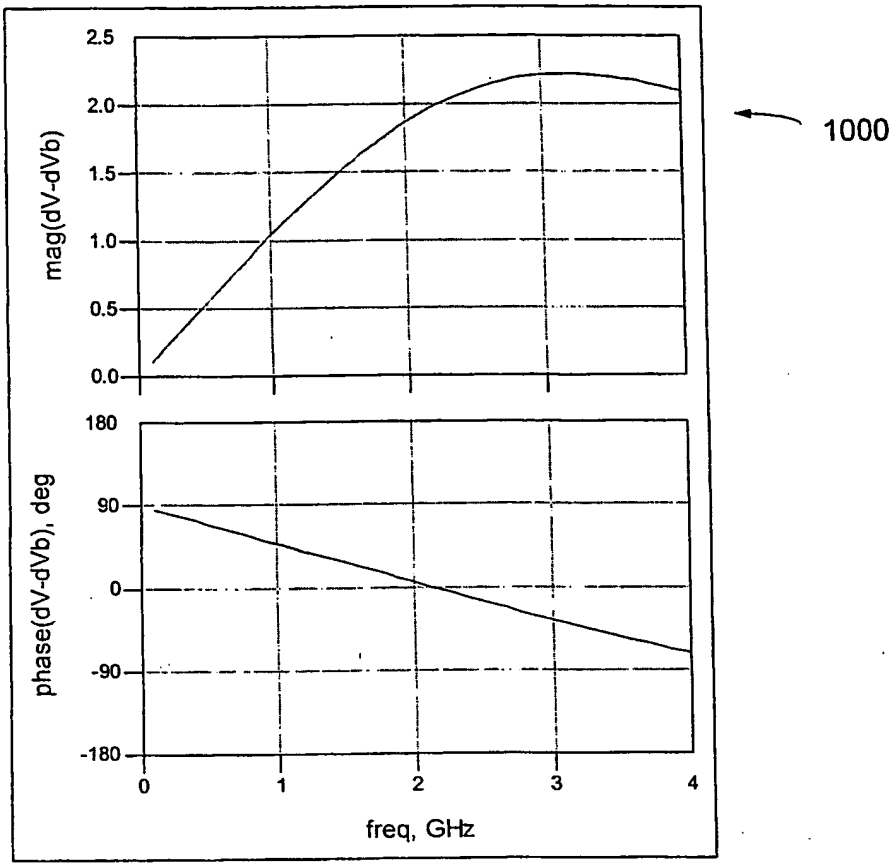
2.5
2.0
1.5
1.0
0.5
0.0
mag(dV-dVb)
180
90
0
-90
-180
phase(dV-dVb), deg
0
1
2
3
4
freq, GHz
1000

FIG. 10

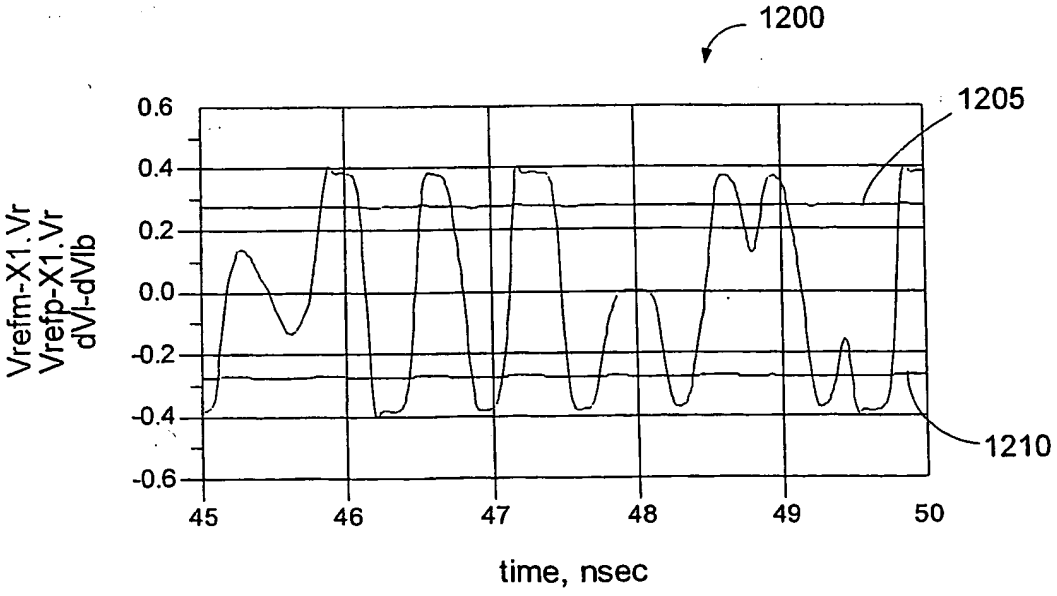
1200
1205
1210
0.6
0.4
0.2
0.0
-0.2
-0.4
-0.6
Vrefm-X1.Vr
Vrefp-X1.Vr
dVl-dVlb
45
46
47
48
49
50
time, nsec

FIG. 12

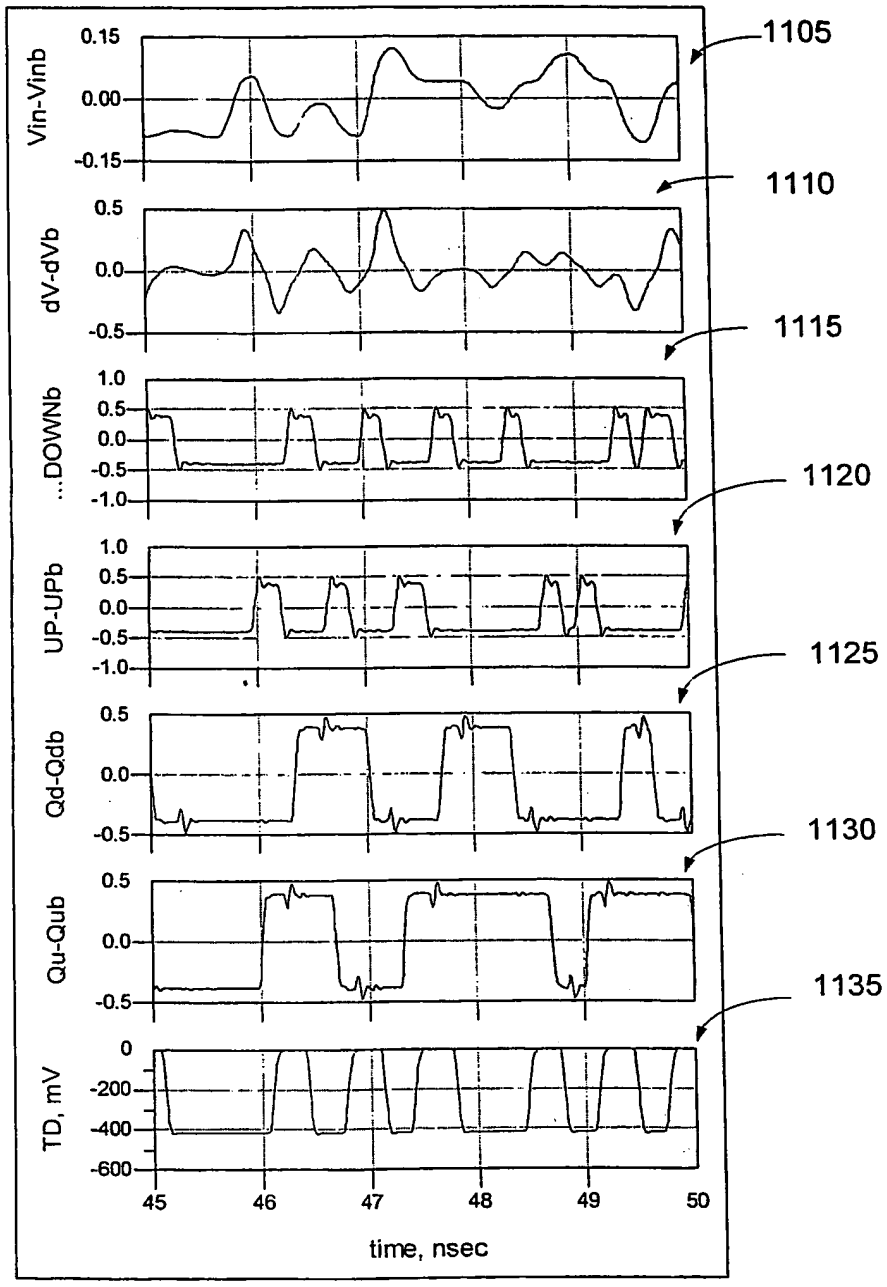
Vin-Vinb
0.15
0.00
-0.15
1105
dV-dVb
0.5
0.0
-0.5
1110
...DOWNb
1.0
0.5
0.0
-0.5
-1.0
1115
UP-UPb
1.0
0.5
0.0
-0.5
-1.0
1120
Qd-Qdb
0.5
0.0
-0.5
1125
Qu-Qub
0.5
0.0
-0.5
1130
TD, mV
0
-200
-400
-600
1135
45
46
47
48
49
50
time, nsec

FIG. 11

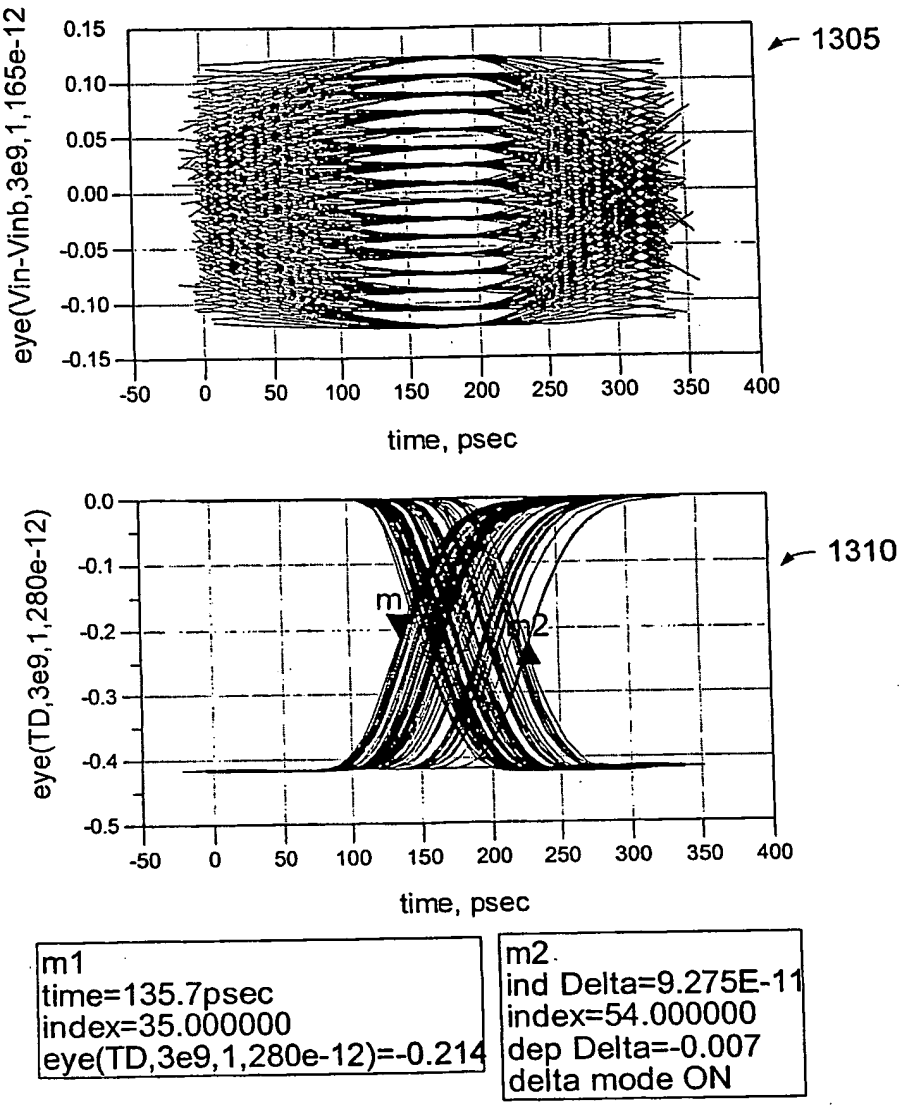
eye(Vin-Vinb,3e9,1,165e-12)
0.15
0.10
0.05
0.00
-0.05
-0.10
-0.15
-50 0 50 100 150 200 250 300 350 400
time, psec
1305
eye(TD,3e9,1,280e-12)
0.0
-0.1
-0.2
-0.3
-0.4
-0.5
-50 0 50 100 150 200 250 300 350 400
time, psec
1310
m
m2
m1
time=135.7psec
index=35.000000
eye(TD,3e9,1,280e-12)=-0.214
m2
ind Delta=9.275E-11
index=54.000000
dep Delta=-0.007
delta mode ON

*FIG. 13*

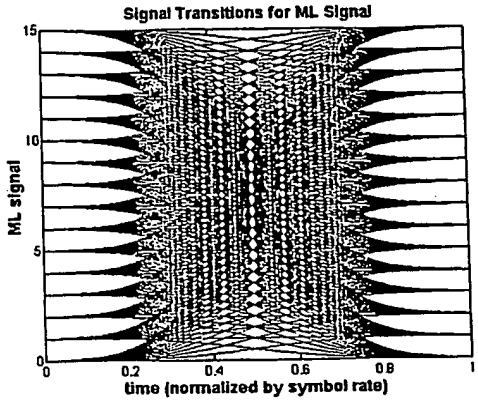


FIG. 14(a)

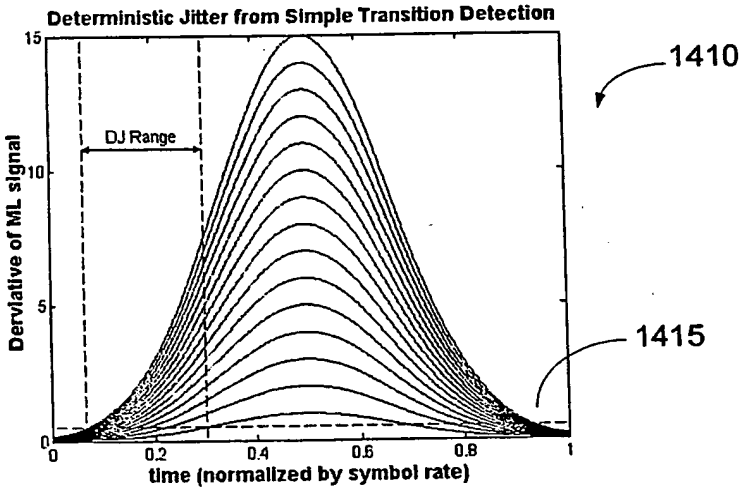


FIG. 14(b)

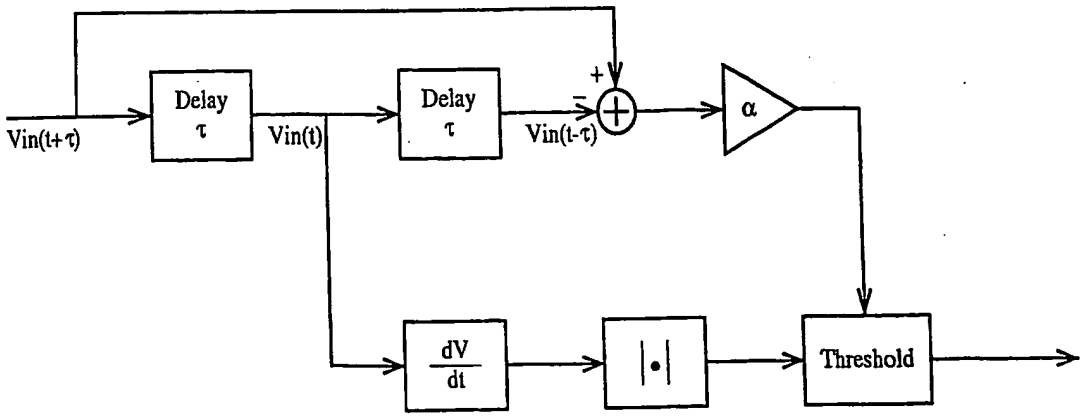


FIG. 15

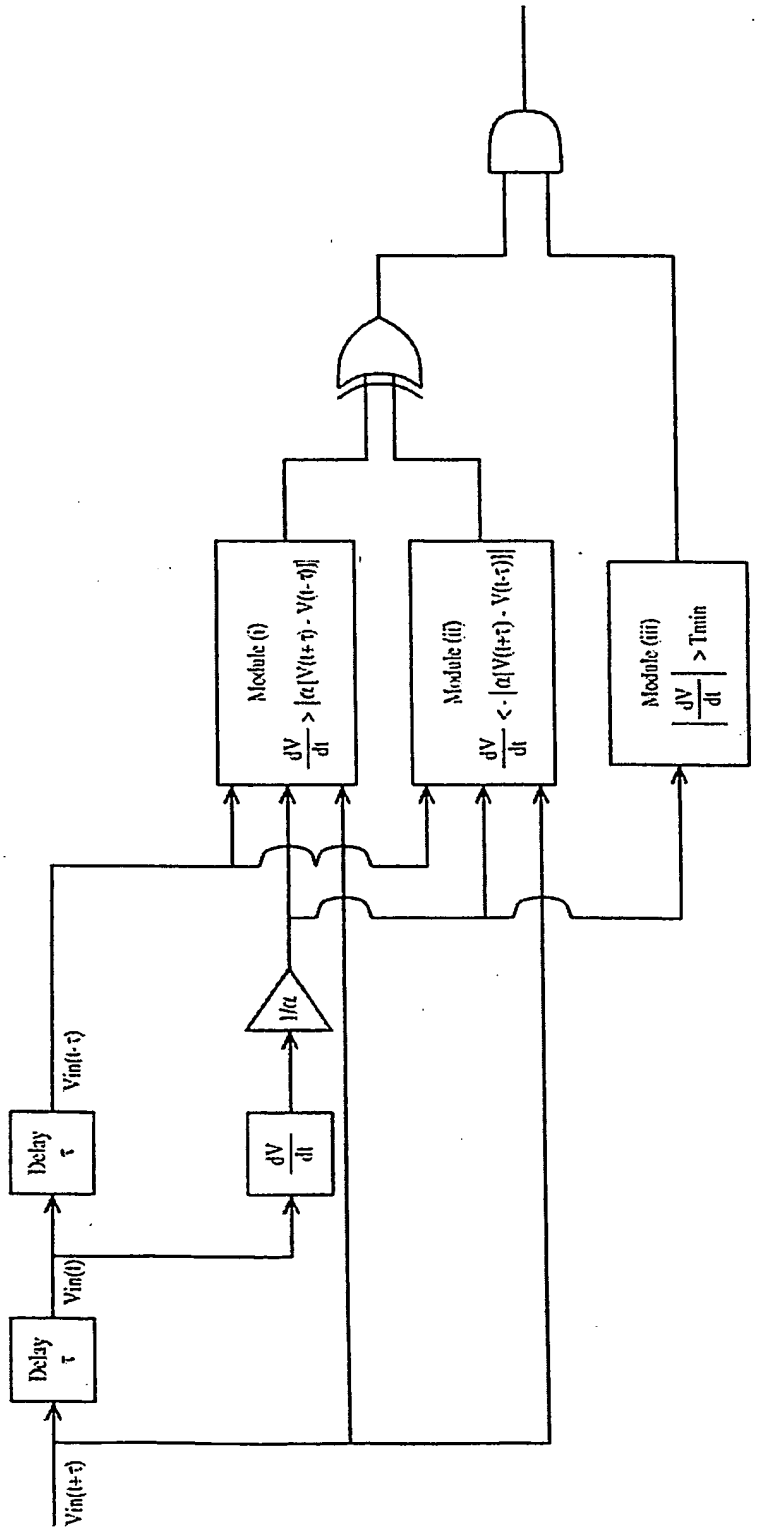
Vin(t+τ)
Delay τ
Vin(t)
Delay τ
Vin(t-τ)
dV/dt
1/α
Module (i)
dV/dt > |α[V(t+τ) - V(t-τ)]|
Module (ii)
dV/dt < -|α[V(t+τ) - V(t-τ)]|
Module (iii)
|dV/dt| > Tmin

Fig. 16

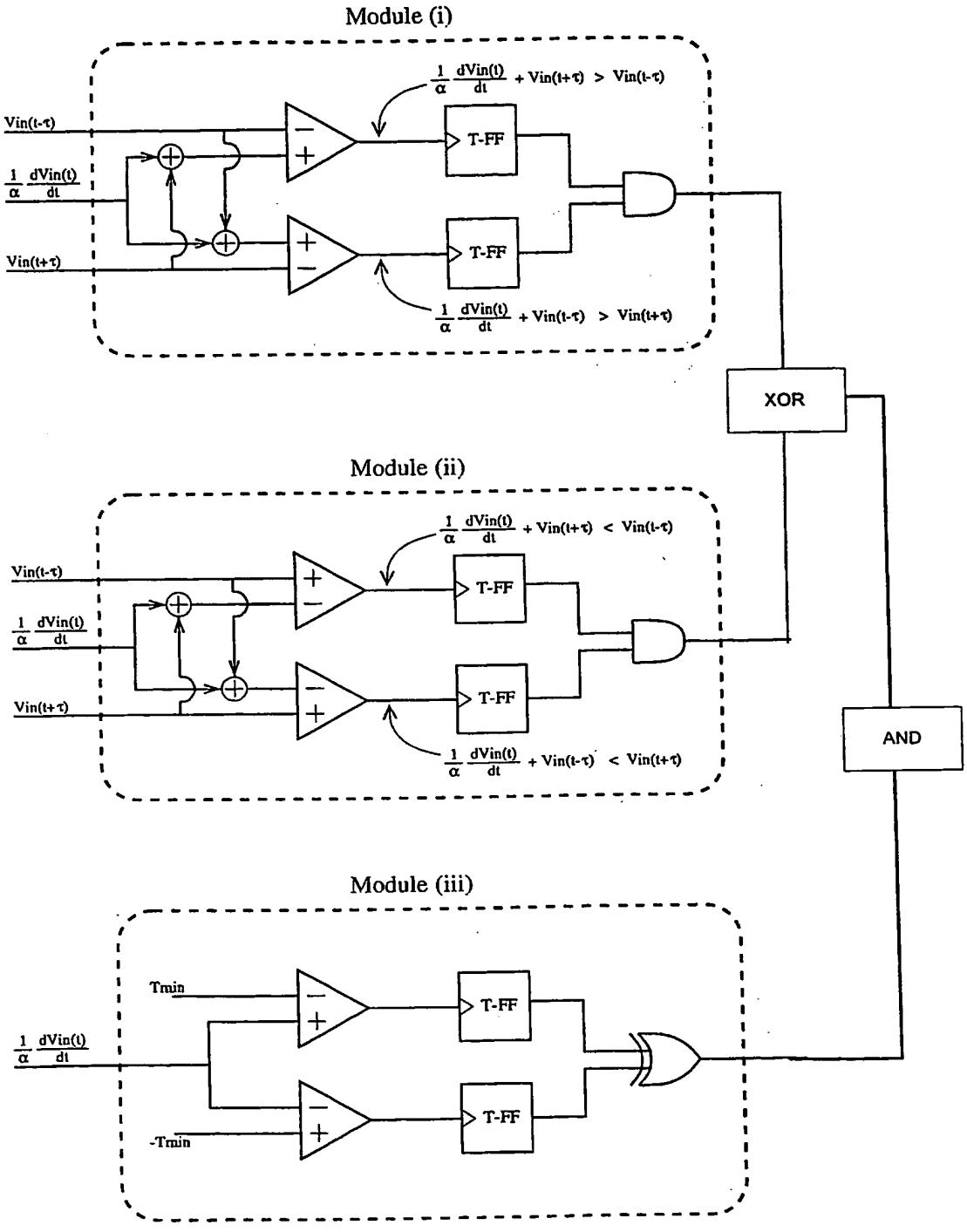
Module (i)
$\frac{1}{\alpha}\frac{dVin(t)}{dt} + Vin(t+\tau) > Vin(t-\tau)$
Vin(t-τ)
$\frac{1}{\alpha}\frac{dVin(t)}{dt}$
Vin(t+τ)
T-FF
T-FF
$\frac{1}{\alpha}\frac{dVin(t)}{dt} + Vin(t-\tau) > Vin(t+\tau)$
XOR
Module (ii)
$\frac{1}{\alpha}\frac{dVin(t)}{dt} + Vin(t+\tau) < Vin(t-\tau)$
Vin(t-τ)
$\frac{1}{\alpha}\frac{dVin(t)}{dt}$
Vin(t+τ)
T-FF
T-FF
$\frac{1}{\alpha}\frac{dVin(t)}{dt} + Vin(t-\tau) < Vin(t+\tau)$
AND
Module (iii)
Tmin
$\frac{1}{\alpha}\frac{dVin(t)}{dt}$
-Tmin
T-FF
T-FF

FIG. 17